Claims

What is claimed is:

1. A processor comprising:

controller circuitry operative to control performance monitoring for at least one flow of protocol data units received by the processor;

the controller circuitry comprising a classifier and being operative to access memory circuitry associated with the processor;

wherein the classifier is configured to perform at least a first pass classification of at least a subset of the protocol data units;

the controller circuitry in conjunction with a first pass classification of a protocol data unit of a first type being operative to execute a first script, and in conjunction with a first pass classification of a protocol data unit of a second type being operative to execute a second script different than the first script, a result of execution of at least one of the first and second scripts being storable in the memory circuitry;

wherein a performance monitoring output is generated, responsive to receipt of the protocol data unit of the second type, based at least in part on the result of execution of at least one of the first and second scripts.

2. The processor of claim 1 wherein the performance monitoring output is generated in conjunction with a second pass classification of the protocol data unit of the second type.

3. The processor of claim 1 wherein in conjunction with a second pass classification of the protocol data unit of the second type, the controller circuitry is further operative to execute a function or other type of script, this additional execution causing the retrieval of a result of execution of the second script from the memory circuitry, the performance monitoring output being generated based at least in part on the result of execution of the second script.

4. The processor of claim 1 wherein the controller circuitry further comprises a compute engine and a traffic manager, the compute engine being operative to execute the first and second scripts, and the traffic manager being operative to generate the performance monitoring output based at least in part on the results of execution the first and second scripts.

5. The processor of claim 1 wherein the protocol data unit of the first type comprises a user protocol data unit, and the protocol data unit of the second type comprises a forward performance monitoring (FPM) protocol data unit.

6. The processor of claim 1 wherein the performance monitoring output comprises a backwards reporting (BR) protocol data unit.

7. The processor of claim 1 wherein at least one of the protocol data units comprises an asynchronous transfer mode (ATM) cell.

8. The processor of claim 1 wherein the performance monitoring is performed in a manner compliant with an I.610 protocol.

9. The processor of claim 1 wherein the first script when executed causes the controller circuitry to increment a count of a plurality of protocol data units of the first type.

10. The processor of claim 1 wherein the first script when executed causes the controller circuitry to generate accumulated parity information over a plurality of protocol data units of the first type.

11. The processor of claim 1 wherein the second script when executed causes the controller circuitry to calculate a backwards reporting (BR) result based at least in part on a result of execution of the first script.

12. The processor of claim 11 wherein the BR result is storable in a circular first-in first-out (FIFO) portion of the memory circuitry.

13. The processor of claim 12 wherein in conjunction with a second pass classification of the protocol data unit of the second type, the controller circuitry is further operative to execute an additional function or other type of script, the additional execution causing the retrieval of the BR result from the circular FIFO portion of the memory circuitry.

14. The processor of claim 13 wherein the performance monitoring output is generated utilizing the protocol data unit of the second type and the retrieved BR result.

15. The processor of claim 11 wherein the BR result indicates how many protocol data units of the first type have been received, up to the time of receipt of a protocol data unit of the second type, since receipt of a previous protocol data unit of the second type.

16. The processor of claim 11 wherein the BR result indicates if any errors are present in the protocol data units of the first type.

17. The processor of claim 11 wherein the BR result is utilized to compute statistics for the flow, the statistics being storable on a per-flow basis in a portion of the memory circuitry.

18. The processor of claim 1 wherein the memory circuitry comprises an external memory of the processor.

19. The processor of claim 1 wherein the processor is configured to provide an interface for communication of the received protocol data units between a network and a switch fabric.

20. The processor of claim 1 wherein the processor comprises a network processor.

21. The processor of claim 1 wherein the processor is configured as an integrated circuit.

22. A method for use in a processor comprising controller circuitry operative to control performance monitoring for at least one flow of protocol data units received by the processor, the controller circuitry comprising a classifier and being operative to access memory circuitry associated with the processor, wherein the classifier is configured to perform at least a first pass classification of at least a subset of the protocol data units, the method comprising the steps of:

executing a first script in conjunction with a first pass classification of a protocol data unit of a first type;

executing a second script different than the first script in conjunction with a first pass classification of a protocol data unit of a second type;

storing a result of execution of at least one of the first and second scripts in the memory circuitry; and

generating a performance monitoring output, responsive to receipt of the protocol data unit of the second type, based at least in part on the result of execution of at least one of the first and second scripts.

23. An article of manufacture comprising a machine-readable storage medium having program code stored thereon for use in a processor comprising controller circuitry operative to control performance monitoring for at least one flow of protocol data units received by the processor, the controller circuitry comprising a classifier and being operative to access memory circuitry associated with the processor, wherein the classifier is configured to perform at least a first pass classification of at least a subset of the protocol data units, the program code when executed in the processor implementing the steps of:

executing a first script in conjunction with a first pass classification of a protocol data unit of a first type;

executing a second script different than the first script in conjunction with a first pass classification of a protocol data unit of a second type;

storing a result of execution of at least one of the first and second scripts in the memory circuitry; and

generating a performance monitoring output, responsive to receipt of the protocol data unit of the second type, based at least in part on the result of execution of at least one of the first and second scripts.